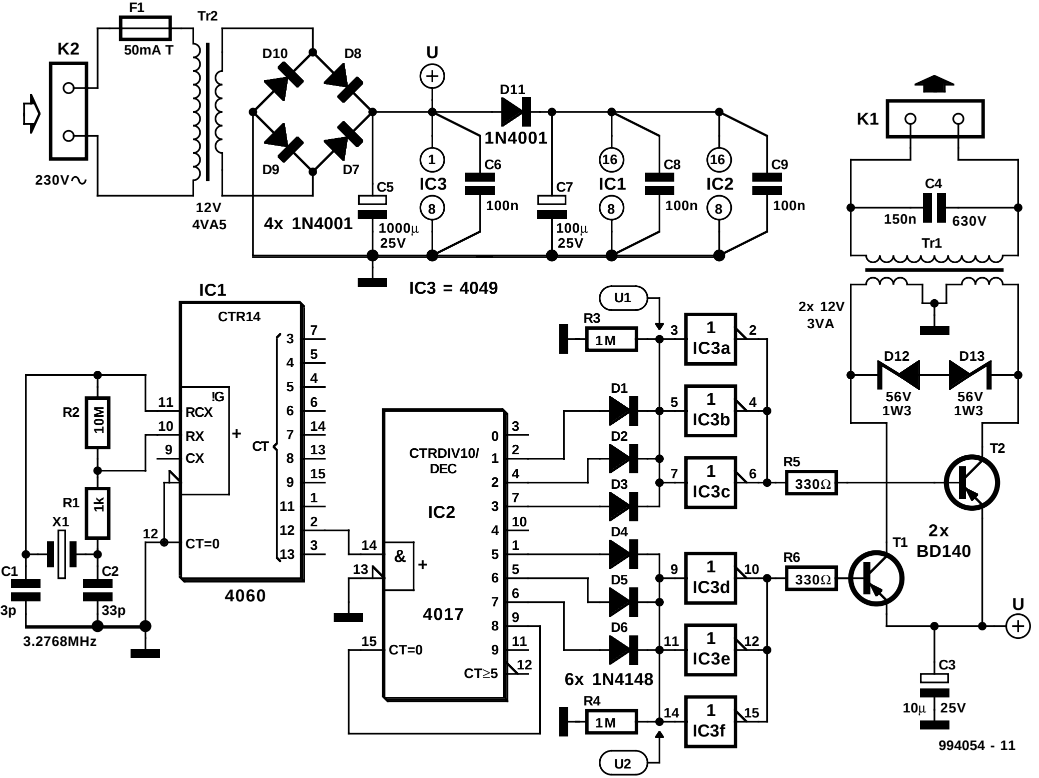
frequency converter

007



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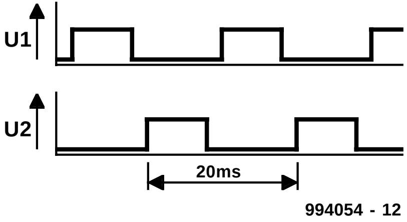
The converter enables a mains voltage with unstable frequency to be converted to one with quartz-crystal stability. It may also be used to convert the mains frequency from 50 Hz to 100 Hz or to 25 Hz. It enables low-power equipment that needs an accurate mains voltage frequency to be supplied from an inexpensive 230 V inverter (driven, say, by a 12 V car battery).

The time base, IC$_1$, of the converter is a crystal oscillator operating with a 3.2768 Mhz quartz crystal. This frequency is divided internally by 2^{13} to give an output frequency of 400 Hz. The 400 Hz signal is applied to counter/divider IC$_2$. When the reset of this IC is linked to Q$_8$ (pin 9), the circuit operates as an :8 divider so that its output is exactly 50 Hz.

The output signals of IC_2 are bundled by wired-OR gates D_1–D_3 and D_4–D_6 into U_1 and U_2 respectively. These signals (shown at the top of Figure 1) are used to control drivers T_1 and T_2 via parallel-connected inverters contained in IC_3, a Type 4049 CMOS circuit. The drivers alternately switch a 12 V transformer winding into circuit, which, because of the constantly changing magnetic flux, results in a stable 230 V alternating voltage across the primary of the transformer.

The drivers are standard Type BD140 p-n-p transistors, so that the inverters in IC_3 draw current when the the relevant driver is on. It is a well-known fact that CMOS elements are far better in drawing current than providing current. The drivers are protected against high-voltage spikes by zener diodes D_{12} and D_{13}.

Capacitor C_4, in conjunction with the stray inductance of the transformer, forms a bypass for high-frequency components in the primary winding of the transformer.



The frequency of the output voltage may be changed to 100 Hz or 25 Hz by linking Q_{11} (pin 1) or Q_{13} (pin 3) respectively to the clock input of IC_2.

Note that in the supply circuit at the bottom of the diagram, diode D_{11} and capacitor C_7 prevent excessive voltage fluctuations caused by the heavy load presented by the drive circuit from adversely affecting the operation of IC_1 and IC_2.

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